

Customer No.: 31561
Docket No.: 7558-US-PA
Application No.: 10/064,916

REMARKS

Present Status of the Application

Upon entry of the amendments in this response, claims 1-7 and 10-16 are pending of which claims 1, 4, 6 and 7 have been amended, and the claims 8 and 17 have been cancelled because they are identical to the claims 5 and 14, respectively, without prejudice or disclaimer in order to more explicitly describe the claimed invention. It is believed that no new matter is added by way of amendments made to the claims. For at least the foregoing reason, applicants respectfully submit that claims 1-7 and 10-16 patentably define over prior art of record and reconsideration of this application is respectfully requested.

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Discussion for objection to claims due to informalities

1. Claims 1-8 and 14 are objected to because of the following informalities

In response thereto, applicants appreciate the examiner's point out the claims' informalities and thus amended all informalities present in claims 1-8 and 14, as instructed by the examiner. The phrases of "having the total memory capacity" as claimed in the claim 1, of "type non-volatile memory second" as claimed in the claim 4 and the adding "at least one" as claimed in the claim 14 are all amended as instructed by the examiner. Besides, the base claim of the claims 7 and 16 are renumbered to make them have proper dependency. Accordingly, it is believed that no informality exists in the claims.

Discussion for objection to claims under 35 U.S.C. 112 2nd Paragraph

3. Claims 6-8 and 15-17 are rejected under 35 U.S.C. 112, 2nd Paragraph, as being indefinite for failing to particularly pointing out and distinctly claim the subject matter which applicant regards as the invention.

In response thereto, applicants found that the claim 8 and 17 are identical to the claims 5 and 14, respectively, and thus cancelled the claims 8 and 17. Moreover, the claims 6-7 and 15-16 were so amended in response to the examiner's objections as follows.

In re claim 6, the text of "the accessed data comprises data stored in segments in one of the second type non-volatile memory device and the replacement memory area other than segments

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replaced by the first type non-volatile memory device, and data stored in the first type non-volatile memory device" is not support by the specification and thus deleted for preventing ambiguity. Meanwhile, the preceding deleted text is replaced with the Fig.2 of the embodiment of the present invention.

In re claim 7, the base claim of the claims 7 is renumbered to the claim 5 so that there exists any antecedent basis for the text of the claims 7.

In re claim 8, as the claim 8 has been cancelled, no argument is needed in this response.

Likewise, the preceding arguments apply to the claims 15-17.

Discussion for rejection to claims under 35 U.S.C.102 (b)

9. Claims 1 and 10 are rejected under 35 U.S.C.102 (b) as being anticipated by Bowers (U.S. Patent 6,233,147 B1)

In response thereto, applicant respectfully traverses the preceding rejection based on the following arguments and thus withdrawal of objections to the claims 1 and 10 is respectfully requested.

To establish a prima facie case of anticipation, the cited reference (i.e. Bowers) should teach all limitations of the amended claims 1 and 10. The examiner alleged that in Bowers, there discloses pin layout for a flash memory (see Fig.3) and an EPROM as disclosed in the claims 1 and 10. Furthermore, the examiner added that the claims 1 and 10 do not require the first and the second memory be in the multi-memory architecture at the same time. However, from the claim

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1 in Bowers, it claims a chip socket for receiving a first chip type or a second chip type; that is, this chip socket is not able to support multi-chip at the same time. In contrast, in the present invention, as obviously seen from Figs.1-2, 5 and 7-9, the first type non-volatile memory device and the second type non-volatile memory device are disposed in the multi-memory architecture at the same time. The claims 1 and 10 are accordingly amended. Therefore, Bowers fails to teach, suggest or disclose "the first type non-volatile memory device and the second type non-volatile memory device are disposed in the multi-memory architecture at the same time," as claimed in the amended claims 1 and 10. In other words, the amended claims 1 and 10 are not anticipated by Bowers and thus patentable.

Regarding to dependent claims 2-7 and 11-16, they should be patentable as a matter of law for the reason that they contain all limitations of their patentable corresponding base claims 1 and 10.

As to claims 6-7 and 15-16, in the "REMARKS" as stated in page 5 in this final rejection notice, the examiner alleged that no prior art has been applied to them due to the ambiguities in the claims as set forth in the rejection of the claims under 35 U.S.C. 112, 2nd paragraph. In this regard, applicants accordingly amended the claims 6-7 and 15-16 so as to. Additionally, applicant respectfully submits that Bowers fails to disclose all limitations taught in the claims 6-7 and 15-16, each of which is believed to particularly pointing out and distinctly claiming the subject matter which applicant regards as the invention.

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CONCLUSION

For at least the foregoing reasons, it is believed that the pending claims 1-7 and 10-16 of the present application patently define over the prior art and are in proper condition for allowance. If the Examiner believes that a telephone conference would expedite the examination of the above-identified patent application, the Examiner is invited to call the undersigned.

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Respectfully submitted,

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